Claims

1. Substrate for EUV microlithography, comprising a base layer and at least one covering layer, the base layer having a coefficient of thermal expansion of at most 0.1 ppm/°C and the covering layer having a coefficient of thermal expansion of at most 1 ppm/°C.

2. Substrate according to Claim 1, in which the covering layer has a thickness of 0.01 to 100 µm.

3. Substrate according to claim 1, in which the covering layer has a surface roughness of at most 0.5 nm rms.

4. Substrate for EUV microlithography, comprising a base layer and at least one covering layer, in which the base layer comprises ceramic and/or glass-ceramic and the covering layer comprises silicon dioxide.

5. Substrate according to Claim 4, in which the base layer comprises Zerodur®, Zerodur® M, Clearceram®, Clearceram® Z or cordierite-containing ceramics.

6. Substrate according to claim 5, in which the covering layer comprises doped silicon dioxide.

7. Substrate according to Claim 6, in which the covering layer comprises TiO_2, other metal oxides, F and/or a mixture of these components as dopants.

8. Substrate according to claim 4, in which the covering layer has a thickness of 0.01 to 100 µm.

9. Process for producing a substrate wherein the substrate comprises at least one covering layer and at least one base layer, the base layer having a coefficient of thermal expansion of at most 0.1 ppm/°C

and the covering layer having a coefficient of thermal expansion of at most 1.0 ppm/°C,

wherein the process comprises the steps of

a) providing a base layer which has a coefficient of thermal expansion of at most 0.1 ppm/°C,

(b) applying a covering layer which has a coefficient of thermal expansion of at most 1.0 ppm/°C, and

(c) if appropriate, polishing the covering layer.

10. Process according to Claim 9, in which the covering layer is applied by a CVD process, in particular a PECVD, PACVD or PICVD process.

11. Process according to Claim 9, in which the covering layer is aftertreated by an IBF process.

12. Process according to of Claim 9, in which the covering layer is applied in a layer thickness of 0.01 µm to 100 µm.

13. An element for EUV microlithography, comprising a substrate and a reflective layer, provided on the substrate;

wherein the substrate comprises at least one covering layer and at least one base layer, the base layer having a coefficient of thermal expansion of at most 0.1 ppm/°C and the covering layer having a coefficient of thermal expansion of at most 1.0 ppm/°C.

14. Element according to Claim 13, wherein the reflective layer is a multilayer.

15. Element according to Claim 14, wherein the reflective layer comprises alternating layers of Mo and Si.

16. Element according to Claim 13, wherein the element is a mirror for EUV microlithography.

17. Element according to Claim 13, wherein the element is a mask or mask blank for EUV microlithography.

18. Element according to Claim 17, further comprising an absorbing layer, provided on the reflective layer.

19. A process of producing an element for EUV microlithography, wherein the element comprises a substrate and a reflective layer, provided on the substrate; and wherein the substrate comprises at least one covering layer and at least one base layer, the base layer having a coefficient of thermal expansion of at most 0.1 ppm/°C and the covering layer having a coefficient of thermal expansion of at most 1.0 ppm/°C;

the process comprising the steps of

(A) providing at least one base layer which has a coefficient of thermal expansion of at most 0.1 ppm/°C,

(B) applying at least one covering layer which has a coefficient of thermal expansion of at most 1.0 ppm/°C,

(C) if appropriate, polishing the covering layer, and

(D) providing a reflective layer on the covering layer of the substrate.

20. A substrate for precision components comprising a base layer and at least one covering layer, the base layer having a coefficient of thermal expansion of at most 0.1 ppm/°C and the covering layer having a coefficient of thermal expansion of at most 1 ppm/°C; wherein the surface roughness of the covering layer is at most 1 nm rms.